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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,949	06/27/2003	Howard Levy	004-8850	3054
22120	7590	01/07/2005	EXAMINER	
ZAGORIN O'BRIEN GRAHAM LLP			TAN, VIBOL	
7600B N. CAPITAL OF TEXAS HWY.			ART UNIT	
SUITE 350			PAPER NUMBER	
AUSTIN, TX 78731			2819	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. Claims 1, 5, 16, 17, and 25 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added recitation of "from a first non-zero strength level to a second non-zero strength level" is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art. It is noted in paragraph [1007] the applicant talks about the reduction in the effective strength of the keeper circuit occurs before arrival of the fastest signal coupled to a sensitive output of the evaluation circuit and the effective strength is restored after arrival of the slowest signal coupled to the sensitive output of the evaluation circuit. However, the applicant never mentions anything relating to a first non-zero strength level and a second non-zero strength level.

The newly added recitations of "an earliest signal" in claim 16 and "a latest signal" in claim 17, respectively, are also not found in the specification.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 18 recites the limitation "the first keeper device" in line 2. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-9, 15, 19-23, 25-27, 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Karnik et al. (U. S. PAT. 6,366,132).

In claim 1, Karnik et al. teaches all claimed features in Fig. 8, a keeper circuit for a dynamic node (N40) of a circuit, wherein the effective strength of the keeper circuit (T40, T41, I7) operating on the dynamic node is reduced during an interval (half of a cycle) in which at least one path in an evaluation circuit (64) is sensitive to a keeper device (T40).

In claims 2-3, Karnik et al. further teaches the circuit of claim 1, wherein the sensitivity of the at least one path includes output of an incorrect value of the evaluation circuit output (noise); wherein a response to the sensitivity is otherwise a reduced speed of the evaluation circuit output (slowing down the speed of the circuit).

In claim 5, Karnik et al. teaches all claimed features in Fig. 8, a circuit comprising: a dynamic node (N40); an evaluation circuit (64) coupled to the dynamic node and a keeper circuit (T40, T41, I7) coupled to the dynamic node.

In claims 6 and 7, Karnik et al. further teaches the circuit of claim 5, wherein the keeper circuit latches an output (input to I5) of the circuit; and wherein the keeper circuit includes a first keeper device (T40).

In claim 8, Karnik et al. further teaches the circuit of claim 7, wherein the keeper circuit includes a keeper gating device (T41) coupled to the first keeper device (T40) and the dynamic node (N40).

In claim 9, Karnik et al. further teaches the circuit of claim 5, wherein the keeper circuit includes a weak keeper device (col. 5, line 65).

In claim 15, Karnik et al. teaches all claimed features in Fig. 8, the circuit of claim 7 wherein the first keeper is sized (col. 5, line 65) to sufficiently overcome the leakage current in the evaluation circuit (greater switching speed).

In claim 19, Karnik et al. further teaches the circuit of claim 5, wherein the dynamic node (N40) is precharged high (Vdd).

In claim 20, Karnik et al. further teaches the circuit of claim 19, wherein the evaluation circuit (64) is n-logic (NMOS PULL-DOWN NETWORK).

In claim 21, Karnik et al. further teaches in Fig. 9, the circuit of claim 5, wherein the dynamic node (N40) is precharged low (to ground when T44 is on).

In claim 22, Karnik et al. further teaches in Fig. 9, the circuit of claim 5, wherein the evaluation circuit (94) is p-logic (p-stack).

Method claim 23 corresponds to detailed circuitry already discussed similarly regard to apparatus claim 5.

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Method claims 25 and 26 correspond to detailed circuitry already discussed similarly regard to apparatus claim 1.

Claim 27 corresponds to detailed circuitry already discussed similarly regard to apparatus claim 5.

In claim 35, Karnik et al. further teaches the circuit of claim 23, wherein the dynamic node (N40) is protected by at least a weak keeper (T40).

In claim 36, Karnik et al. further teaches the circuit of claim 27, wherein the means for protecting the dynamic node comprises a weak keeper (T40).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karnik et al. in view of Nowka et al. (U. S. PAT. 6,404,235).

In claim 10, Karnik et al. teaches all claimed features the circuit of claim 5; with the exception of teaching wherein the keeper circuit is responsive to a keeper control. However, Nowka et al. teaches in Fig. 2, the keeper circuit (220) is responsive to a keeper control (207).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to make a keeper circuit responsive to a keeper control

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circuit (207), as taught by Nowka et al., in order to further reduce switching latency during the evaluation interval.

9. Claims 13, 14, 29, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karnik et al. in view of the applicant's admitted prior art in Fig. 1.

In claim 29, Karnik et al. teaches all claimed features in Fig. 8, a circuit comprising: a dynamic node (N40); a precharge device (T33) coupled to the dynamic node; an evaluation circuit (64) coupled to the dynamic node; a clock node coupled to the precharge device; and a keeper circuit (T40, T41, I7) coupled to the dynamic node, wherein a first keeper device (T40) is selectively disabled during a first interval (a first transitioning); with the exception of showing a discharge device coupled to the evaluation circuit and the clock node coupled to the discharge device. However, the applicant's admitted prior art in Fig. 1 teaches a discharge device (110) coupled to the evaluation circuit (104-108) and the clock node (CLOCK) coupled to the discharge device.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to include a discharge device in the circuit of Karnik in order to quickly couple the evaluation network stack to ground so the inputs can be evaluated in a timely fashion.

In claim 33, Karnik et al. further teaches the circuit of claim 29, further comprising: a keeper gating device (T41) coupling to the first keeper device (T40) to the dynamic node (N40).



In claim 34, Karnik et al. further teaches the circuit of claim 29, wherein the first keeper has a gain sufficient (col. 5, line 65) to overcome leakage current in the evaluation circuit (greater switching speed).

Claims 13 and 14 basically correspond to detailed circuitry already discussed similarly with regard to claim 29.

10. Claims 30-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Response to Arguments***

11. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1-3, 5-9, 15, 19-23, 25-27, 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Karnik et al., as explained in details above.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karnik et al. in view of Nowka et al.

Claims 13, 14, 29, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karnik et al. in view of the applicant's admitted prior art in Fig. 1.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP



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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan

Primary Examiner, AU 2819



**VIBOL TAN**  
**PRIMARY EXAMINER**